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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,574	03/12/2004	Hoon Kim	P57012	6505

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EXAMINER	
DICKEY, THOMAS L	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,574	KIM, HOON	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *7-12 and 17-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 13-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 09/01/2005 has been entered.

2. Due to the application of a new ground of rejection this action is non-final.

Information Disclosure Statement

3. The Information Disclosure Statement filed on 07/01/2005 has been considered.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 3-6,15, and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. In line 3 of each of claims 3-6, 15, and 16,"polysilicon" has no antecedent basis. It is clear from the claims that each of these "polysilicons" has a thickness and is formed by SPC or ELA methods, as the case may be. What is indefinite is where the antecedent basis of "polysilicon" resides. The specification states that the "activation layer" of claims 1 and 13 is activated by either the ELA or SPC methods, so it seems likely that the antecedent of "polysilicon" is "an activation layer." If this is the case

applicant should spell this out in the claims, using language such as (for example) – wherein said activation layer is formed from SPC polysilicon having a thickness of...–

In the examiner's opinion there is nothing wrong with describing the ELA and SPC methods using their acronyms. There are literally tens of thousands of documents available in the prior art to teach one having skill in the art what these acronyms mean, and how to practice the methods so referred to.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A. Claims 1,2,4,6,13,14, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by BUSTA (4,949,141).

(1) With regard to claims 1,2,4, and 6 Busta discloses a thin film transistor comprising a buffer layer 12-32 formed on a substrate 10; an 8000 angstrom thick (Note column 5 line 9. The thickness of the activation layer 34 must be known to know whether the reference meets the claims) activation layer 34 formed on said buffer layer 12-32; and a gate insulation layer 40 having a thickness of at least 1,000 angstroms (1200-2000 angstroms, see column 5 line 20) formed on said substrate 10 including said activation layer 34, with said buffer layer 12-32 having a 750 angstrom (column 5

line 9 discloses a 500-1500 angstrom range) step 32 (the size of the step 32 is defined by projecting buffer layer part 32. The projecting part and the step 32 it creates will be interchangeably referred to as part "32") formed between a lower part of said activation layer 34 and a part except said lower part of said activation layer 34, said 750 angstrom step 32 being a half or less of the thickness sum (the sum of 8000, activation layer 34, and 1000, gate insulation layer 40, being 9000) of said activation layer 34 and gate insulation layer 40, and further comprising a 500 (500-1500 angstroms, note column 5 line 9) angstrom polysilicon layer 36. Note (figure 2B) that the thickness of the gate insulation layer 40 is not changed on said sidewall of said buffer layer 12-32 (the side wall of the buffer layer 12-32 is the sidewall of the step 32 portion of the buffer layer 12-32). Therefore the buffer layer 12-32 must have a step 32 to such a degree as to accomplish this visible result. Note figure 2B, column 4 lines 50-51, and column 5 lines 9,10, and 20 of Busta.

The applicant's claims 4 and 6 do not distinguish over the Busta reference regardless of the process used to form polysilicon layer 36, because only the final product is relevant, not the recited process of excimer laser annealing (ELA).

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it

is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

(2) With regard to claims 13,14, and 16 Busta discloses a thin film transistor comprising a buffer layer 12-32; an 8000 angstrom thick (Note column 5 line 9. The thickness of the activation layer 34 must be known to know whether the reference meets the claims) activation layer 34 formed on said buffer layer 12-32; and a gate insulation layer 40 having a thickness of at least 1,000 angstroms (1200-2000 angstroms, see column 5 line 20) formed on said buffer layer 12-32 and said activation layer 34, with said buffer layer 12-32 having a 750 angstrom (column 5 line 9 discloses a 500-1500 angstrom range) step 32 (the size of the step 32 is defined by projecting buffer layer 12-32 part 32. The projecting part and the step 32 it creates will be interchangeably referred to as part "32") formed between a lower part of said activation layer 34 and a part except said lower part of said activation layer 34, and said step 32 being up to a half of the thickness sum of said activation layer 34 and gate insulation layer 40. Note (figure 2B) that the thickness of the gate insulation layer 40 is deposited to an even thickness on a side wall of the activation layer 34 Therefore the step 32 must have been controlled (to such extent necessary) as to accomplish this visible result. Note figure 2B, column 4 lines 50-51, and column 5 lines 9,10, and 20 of Busta.

The applicant's claim 16 does not distinguish over the Busta reference regardless of the process used to form polysilicon layer 36, because only the final product is relevant, not the recited process of excimer laser annealing (ELA).

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

B. Claims 1,2,13, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by ADACHI ET AL. (5,985,704).

With regard to claims 1 and 2 Adachi et al. discloses a thin film transistor with a buffer layer 22 (12 in figure 1) formed on a substrate 21 (11); a 1000-1500 angstrom activation layer 13 (23 in figure 2) formed on said buffer layer 22 (12 in figure 1); and a 300 angstrom gate insulation layer 29 formed on said substrate 21 (11) including said activation layer 13 (23 in figure 2), with said buffer layer 22 (12 in figure 1) having a step "y" formed between a lower part of said activation layer 13 (23 in figure 2) and a part

except said lower part of said activation layer 13 (23 in figure 2), the step "y" in the buffer layer 22 (12 in figure 1) having such a degree that thickness of the gate insulation layer 29 is not changed on said side wall of said buffer layer 22 (12 in figure 1) and being 80-500 angstroms thick and thus a half or less of the thickness sum (1000-1500 plus 300 angstroms) of said activation layer 23 (1000-1500 angstroms thick) and gate insulation layer 29(300 angstroms thick). Note figures 1A-1E, 2A-E, column 4 lines 1-5 and 20-24, and column 8 lines 1-5,18-24, and 41-55 of Adachi et al.

With regard to claims 13 and 14 Adachi et al. discloses a thin film transistor with a buffer layer 22 (12 in figure 1); a 1000-1500 angstrom activation layer 13 (23 in figure 2) formed on said buffer layer 22 (12 in figure 1); a 300 angstrom gate insulation layer 29 formed on said buffer layer 22 (12 in figure 1) and said activation layer 13 (23 in figure 2), with said buffer layer 22 (12 in figure 1) having a step "y" controlled according to said gate insulation layer 29 deposited to an even thickness on a side wall of said activation layer 13 (23 in figure 2), and formed between a lower part of said activation layer 13 (23 in figure 2) and a part except said lower part of said activation layer 13 (23 in figure 2), said step "y" being 80-500 angstroms thick and thus up to a half of the thickness sum (1000-1500 plus 300 angstroms) of said activation layer 23 (1000-1500 angstroms thick) and gate insulation layer 29(300 angstroms thick). Note figures 1A-1E, 2A-E, column 4 lines 1-5 and 20-24, and column 8 lines 1-5,18-24, and 41-55 of Adachi et al.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

C. Claims 3,5, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over ADACHI ET AL. (5,985,704) in view of YAMAZAKI ET AL. (2004/0211356).

Adachi et al. discloses a thin film transistor with all the limitations of claims 3,5, and 15, including that the step be 350 angstroms (Adachi et al. disclose 80-500 angstroms) in the activation layer, except that the thickness of the gate insulation layer be at least 400 (400 angstroms or more) angstroms and that the activation layer comprise polysilicon having a thickness of 300 angstroms. Note figures 1A-1E, 2A-E, column 4 lines 1-5 and 20-24, and column 8 lines 1-5,18-24, and 41-55 of Adachi et al.

However, Yamazaki et al. discloses a thin film transistor with that a thickness of a gate insulation layer 405 that is 400 angstroms or more (1000-1500 angstroms) and an activation layer 403 comprising KrF excimer laser activated polysilicon having a thickness of 300 angstroms. Note figures 7A-D, 10A-C, and paragraphs 0088-0098 of Yamazaki et al. Therefore, it would have been obvious to a person having skill in the art to modify the dimensions of the of Adachi et al.'s thin film transistor to the dimensions taught by Yamazaki et al. in order to increase gate-channel breakdown voltage by

thickening the gate insulating film, while at the same time making it easier to fully deplete the channel, by making the channel shallower, to thus provide a TFT able to perform over a wider range of voltages.

Response to Arguments

6. Applicant's arguments filed 09/01/05 have been fully considered but they are not persuasive.

It is argued, at page 10 of the remarks, that "Therefore, reference 32 can be included as the activation layer rather than the buffer layer as the buffer layer is stated in the claim as not being the activation layer." In context it is clear that applicant is using "can" as permissive. "Can be," means "may be," or "could be," in this vernacular. However, patent claims construed during examination should be given their broadest reasonable interpretation consistent with specification, since this policy serves public interest by reducing possibility that claims, finally allowed, will be given broader scope than is justified (In re American Academy of Science Tech Center, 70 USPQ2d 1827, Decided May 13, 2004). The broadest reasonable interpretation of a claim term that may mean "X" or, on the other hand, may mean "Y," is to assume the claim term means "X or Y." Therefore for examination purposes it will be assumed reference 32 may be included in either the buffer layer or the activation layer.

It is argued, at page 11 of the remarks, that "However, layer 32 is the drain layer which can still be categorized as the activation layer and not the buffer layer." The same

reasoning is applicable to "can still be categorized," as was just applied to "can be included." It means, "May, but not necessarily must, be categorized."

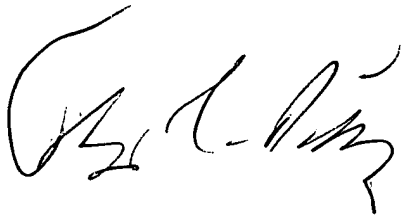
It should be noted that Busta discloses a TFT designed for vertical current flow, as opposed to lateral flow. The Adachi and Yamazaki TFTs are lateral TFTs. However, as Adachi points out, a 500-angstrom step is an extremely tall step for a lateral TFT. Without extreme care laying down the gate insulating layer (for example, laying down two or more separate insulating layers) a short may be generated at the side surface of the activation layer when the buffer layer is etched so deeply as to make a 500-angstrom step. Yet applicant's claims 4, 6, and 16 require a 750-angstrom step. To accomplish such a very extreme step, it is safer to build a vertical TFT, such as taught by Busta, where the gate, and the gate insulator, is essentially laid down on the side of the step.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Patent Examiner
Art Unit 2826
10/05